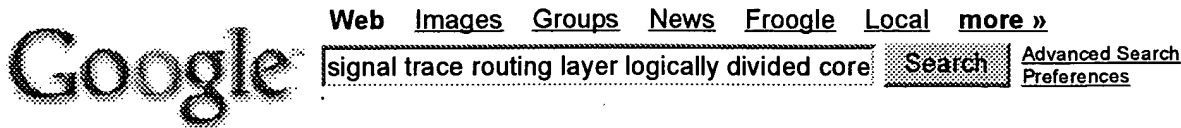


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L1	1266	core and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:01
L2	883	1 and via\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:00
L3	282	(core same (divid\$3 or section or logical\$3)) and "716"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:02
L4	190	3 and via\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:27
L5	15882	core and section and logical\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:28
L6	184560	core and section and logical\$2 via and (void or clearance)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:28
L7	2124	core and section and logical\$2 and via and (void or clearance)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:28
L8	1371	core and section and logical\$2 and via and (void or clearance) and contact	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:29
L9	560	core and section and logical\$2 and via and (void or clearance) and contact and ((reference or vdd or gnd or power or ground) same layer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:30

L10	446	core and section and logical\$2 and via and (void or clearance) and contact and ((reference or vdd or gnd or power or ground) same layer) and align\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:30
L11	19	core and section and logical\$2 and via and (void or clearance) and contact and ((reference or vdd or gnd or power or ground) same layer) and align\$3 and ("716"/\$.ccls. or "257"/\$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:31
S65	457	(716/9,15).CCLS.	USPAT; USOCR	OR	OFF	2005/08/01 13:48
S66	565	(716/9,15).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 07:59
S67	8	ramakrishnan-a\$4.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/01 13:50

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L2	1	((substrate or pcb or (printed near2 board)) core (via\$2 or hole) (void or clearance) (reference or vdd or gnd or power or ground) contact (signal or trace or wir\$3 or path or metal) overlying align\$4 row).clm.	US-PGPUB	AND	ON	2005/08/02 10:09



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Scholarly articles for signal trace routing layer logically divided core section contact align via void



Title EGSO Architecture - by Distribution - 0 citations

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The **core** constrains the expansion of the outer **layers** to match the expansion ...
feed-through via A plated-through hole in a PWB used to route a **trace** ...

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Whilst **logically** representing a point to point link between RNCs, the physical
... The protocols over Uu and Iu interfaces are **divided** into two structures: ...

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My third HTPC that drives the projector is connected via SPDIF so it does ...

A simple PCI card with some sort of microcontroller/**signal routing** device (? ...

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Technology could **void** the user's authority to operate the equipment. ...
ground planes, and other **signal routing** on the inner. and surface **layers**. ...

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The logic design for TTL_PAPERS is **logically** (and physically) **divided** into ...
tion where the **signal** is used on the board, a single **layer** suffices for all ...

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Sitting at this **layer**, you might also add an NCP (Netware **Core** Protocol) ...

All entries in the **routing** table are entered via the EZCom-IP explore program. ...

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Railway Lexicon

Block Section The **section** of line between the **section signal** of one **signal** ...
up of conflicting **routes** by **logically** linking points and **signal** operation. ...

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the of to a and is in I that you it for be are have not with on s ...

... sounds reaction directly produced center gamma areas **signal** fit Even symptoms


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substrate traces, the signals may not be aligned at the land pads of the ...
 VOID. = πr . 2. /2. (Eq 2). A. EFFECTIVE. is based on the signal routing layer ...

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quantum size effects. Related activities include an expanded ... improved solutions
 for the channel routing problem and the problem of routing around a ...

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Substrate resistanceand inductance modeling will become important. ... 5C.1 POST
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Routing and distributing the clock signal are only part of the design process.

... It follows that variation in the power supply and substrate voltages will ...

www.eecs.umich.edu/UMichMP/ Publications/Proposals/stetson.ps - [Similar pages](#)**8 OSKit Device Driver (OS Environment) Framework**

Routing all memory allocations through a single interface this way may ...

void *osenv_mem_alloc(oskit_size_t size, osenv_memflags_t flags, unsigned align); ...

www.cs.utah.edu/flux/oskit/html/oskit-wwwch8.html - 166k - [Cached](#) - [Similar pages](#)**Dpt. of Defense SBIR Awards 1994**

Utilization of multi-path and multi-routing capabilities allow highly ...

Problems with this technology include low yields, limited substrate size, ...

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#2 ((core <and> divided <and> vias <and> void)<in>metadat...
#3 ((core <and> via <and> void)<in>metadata)
#4 ((core <and> via <and> void)<in>metadata)
#5 (substrate <and> space <and> size<IN>metadata)

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